WHAT IS CLAIMED IS:

1. A semiconductor component comprising:

a metal leadframe comprising a plurality of leadfingers;

a semiconductor die having a back side attached to the leadframe in a chip on board configuration;

a plurality of interconnects bonded to the die and to the leadframe; and

a plurality of terminal contacts attached to the leadframe in an area array.

2. The semiconductor component of claim 1 and further comprising an encapsulant encapsulating the die, the interconnects and the leadframe.

3. The semiconductor component of claim 1 wherein the terminal contacts comprise bumps or balls in a grid array.

4. The semiconductor component of claim 1 wherein the interconnects comprise wire bonded wires.

5. A semiconductor component comprising:

a leadframe comprising a plurality of leadfingers, a plurality of interconnect bonding sites on a first side thereof and a plurality of terminal bonding sites on a second side thereof in an area array;

a semiconductor die having a back side attached to the leadfingers on the first side;

a plurality of interconnects bonded to the die and to the interconnect bonding sites;

a plurality of terminal contacts on the terminal bonding sites; and

an encapsulant encapsulating the die, the interconnects and the leadframe.

6. The semiconductor component of claim 5 further comprising at least one bus bar electrically connecting selected leadfingers and located to not cross the interconnects.

7. The semiconductor component of claim 5 wherein the interconnects comprise wire bonded wires.

8. The semiconductor component of claim 5 wherein the terminal contacts comprise bumps or balls and the terminal bonding sites are arranged in a grid array.

9. The semiconductor component of claim 5 wherein the leadframe comprises a chip on board leadframe.

10. The semiconductor component of claim 5 further comprising an adhesive member attaching the back side of the die to the leadfingers.

11. The semiconductor component of claim 5 wherein the interconnect bonding sites comprise first metal layers on the leadfingers.

12. The semiconductor component of claim 5 wherein the terminal bonding sites comprise second metal layers on the leadfingers.

13. The semiconductor component of claim 5 wherein the leadframe and the encapsulant have a chip scale outline.

14. A semiconductor component comprising:

a leadframe comprising a plurality of leadfingers, a plurality of interconnect bonding sites on the leadfingers,

a plurality of terminal bonding sites on the leadfingers and at least one bus bar electrically connecting selected leadfingers;

a semiconductor die comprising a circuit side, a plurality of die contacts on the circuit side, and a back side attached to the leadframe;

a plurality of interconnects bonded to the die contacts and to the interconnect bonding sites;

a plurality of terminal contacts on the terminal bonding sites; and

an encapsulant encapsulating the die and the leadframe.

15. The semiconductor component of claim 14 wherein the interconnect bonding sites are located proximate to an outer periphery of the leadframe and the bus bar is located proximate to an inner portion of the leadframe.

16. The semiconductor component of claim 14 wherein the interconnect bonding sites are located relative to the bus bar such that the interconnects do not cross the bus bar.

17. The semiconductor component of claim 14 wherein the interconnects comprise wire bonded wires.

18. The semiconductor component of claim 14 wherein the terminal contacts comprise metal bumps or balls and the terminal bonding sites are arranged in a grid array.

19. The semiconductor component of claim 14 wherein the interconnect bonding sites comprise first metal layers on a first side of the leadfingers and the terminal bonding sites comprise second metal layers on an opposing second side of the leadfingers.

20. A semiconductor component comprising:

a leadframe having a first side, an opposing second side, an inner portion and an outer periphery, the leadframe comprising a plurality of leadfingers;

a plurality of interconnect bonding sites on the leadfingers on the first side located proximate to the outer periphery;

a plurality of terminal bonding sites on the leadfingers on the opposing second side in an area array;

at least one bus bar electrically connecting selected leadfingers located proximate to the inner portion;

a semiconductor die back bonded to the leadfingers on the first side;

a plurality of interconnects bonded to the die and to the interconnect bonding sites; and

a plurality of terminal contacts on the terminal bonding sites.

21. The semiconductor component of claim 20 further comprising an encapsulant encapsulating the die and the leadframe.

22. The semiconductor component of claim 20 wherein the leadframe has a chip on board configuration.

23. The semiconductor component of claim 20 wherein the interconnect comprise wires.

24. The semiconductor component of claim 20 further comprising an adhesive member attaching the die to the first side.

25. The semiconductor component of claim 20 wherein the terminal contacts comprise metal balls or metal bumps.

26. The semiconductor component of claim 20 wherein the leadframe includes a die mounting site on the first side proximate to the inner portion.

27. A semiconductor component comprising:

a leadframe having a first side and an opposing second side, the leadframe comprising a plurality of leadfingers having a die mounting site on the first side, a plurality of interconnect bonding sites on the first side, a plurality of terminal bonding sites on the second side in an area array and a plurality of bus bars electrically connecting selected leadfingers;

a semiconductor die having a back side attached to the die mounting site;

a plurality of interconnects bonded to the die and to the interconnect bonding sites, the interconnect bonding sites and the bus bars located on the leadframe such that the interconnects do not cross the bus bars;

a plurality of terminal contacts on the terminal bonding sites; and

an encapsulant encapsulating the die, the leadframe, and the interconnects.

28. The semiconductor component of claim 27 wherein the interconnect bonding sites are located proximate to an outer periphery of the leadframe and the bus bars are located proximate to an inner portion of the leadframe.

29. The semiconductor component of claim 27 wherein the leadfingers are arranged in rows along opposing sides of the leadframe.

30. The semiconductor component of claim 27 wherein the interconnects comprise wires.

31. The semiconductor component of claim 27 wherein the leadframe has a chip on board configuration.

32. The semiconductor component of claim 27 wherein the encapsulant has a chip scale outline.

33. The semiconductor component of claim 27 wherein the leadframe has a chip scale outline.

34. The semiconductor component of claim 27 wherein the interconnect bonding sites and the terminal bonding sites comprise a metal selected from the group consisting of Al, Cu, Au and alloys thereof.

35. The semiconductor component of claim 27 wherein the die comprises a plurality of die contacts on the circuit side and the interconnects are bonded to the die contacts.

36. The semiconductor component of claim 27 wherein the terminal contacts comprise bumps or balls in a grid array.

37. A method for fabricating a semiconductor component comprising:

providing a metal leadframe having a first side and a second side;

attaching a semiconductor die to the first side in a chip on board configuration;

bonding a plurality of interconnects to the die and to the leadframe; and

forming a plurality of terminal contacts on the leadframe on the second side.

38. The method of claim 37 further comprising forming an encapsulant on the die, on the interconnects and on the leadframe.

39. The method of claim 37 wherein the interconnects comprise wires and the bonding step comprises wire bonding.

40. A method for fabricating a semiconductor component comprising:

providing a chip on board leadframe comprising a plurality of leadfingers, a plurality of interconnect bonding sites on a first side thereof and a plurality of terminal bonding sites on a second side thereof in an area array;

attaching a back of a semiconductor die to the leadfingers on the first side;

bonding a plurality of interconnects to the die and to the interconnect bonding sites;

forming a plurality of terminal contacts on the terminal bonding sites; and

forming an encapsulant on the die, on the interconnects and on the leadframe.

41. The method of claim 40 wherein the attaching step comprises forming an adhesive member between the die and the leadframe.

42. The method of claim 40 wherein the forming the terminal contacts step comprises forming or attaching bumps or balls to the terminal bonding sites.

43. The method of claim 40 wherein the interconnects comprise wires and the bonding step comprises wire bonding.

44. The method of claim 40 wherein the leadframe is contained on a strip containing a plurality of leadframes.

45. A method for fabricating a semiconductor component comprising:

providing a leadframe comprising a plurality of leadfingers, a plurality of interconnect bonding sites on the leadfingers, a plurality of terminal bonding sites on the leadfingers and at least one bus bar electrically connecting selected leadfingers;

providing a semiconductor die comprising a circuit side, a plurality of die contacts on the circuit side, and a back side;

attaching the back side of the die to the leadframe;

bonding a plurality of interconnects to the die contacts and to the interconnect bonding sites without crossing the bus bar with the interconnects;

forming a plurality of terminal contacts on the terminal bonding sites; and

forming an encapsulant on the die and the leadframe.

46. The method of claim 45 wherein the interconnect bonding sites are located proximate to an outer periphery of the leadframe and the bus bar is located proximate to an inner portion of the leadframe.

47. The method of claim 45 wherein the interconnects comprise wires.

48. The method of claim 45 wherein the terminal contacts comprise metal bumps or balls and the terminal bonding sites are arranged in a grid array.

49. The method of claim 45 wherein the leadframe comprises a chip on board leadframe.

50. The method of claim 45 wherein the forming the encapsulant step comprises transfer molding a polymer on the die and the leadframe.

51. A method for fabricating a semiconductor component comprising:

providing a leadframe having a first side, an opposing second side, an inner portion and an outer periphery, the leadframe comprising a plurality of leadfingers, a plurality of interconnect bonding sites on the leadfingers on the first side located proximate to the outer periphery, a plurality of terminal bonding sites on the leadfingers on the opposing second side in an area array and at least one bus bar electrically connecting selected leadfingers located proximate to the inner portion;

attaching a semiconductor die to the leadfingers on the first side;

bonding a plurality of interconnects to the die and to the interconnect bonding sites; and

forming a plurality of terminal contacts on the terminal bonding sites.

52. The method of claim 51 further comprising forming an encapsulant on the leadframe and the die.

53. The method of claim 51 wherein the interconnects comprise wires and the bonding step comprises wire bonding.

54. The method of claim 51 wherein the attaching step comprises forming an adhesive member between the die and the leadframe.

55. The method of claim 51 wherein the forming the terminal contacts step comprises forming or attaching bumps or balls to the terminal bonding sites.

56. The method of claim 51 wherein the leadframe is contained on a strip containing a plurality of leadframes.

57. A method for fabricating a semiconductor component comprising:

providing a leadframe having a first side and an opposing second side, the leadframe comprising a plurality of leadfingers having a die mounting site on the first side, a plurality of interconnect bonding sites on the first side, a plurality of terminal bonding sites on the second side in an area array and a plurality of bus bars electrically connecting selected leadfingers;

back bonding a semiconductor die to the die mounting site;

bonding a plurality of interconnects to the die and to the interconnect bonding sites without crossing the bus bars with the interconnects;

forming a plurality of terminal contacts on the terminal bonding sites; and

encapsulating the die, the leadframe, and the interconnects in an encapsulant.

58. The method of claim 57 wherein the interconnect bonding sites are located proximate to an outer periphery of the leadframe and the bus bars are located proximate to an inner portion of the leadframe.

59. The method of claim 57 wherein the interconnects comprise wires.

60. The method of claim 57 wherein the leadframe has a chip on board configuration.

61. The method of claim 57 wherein the encapsulant has a chip scale outline.

62. The method of claim 57 wherein the leadframe has a chip scale outline.

63. The method of claim 57 wherein the forming the terminal contacts step comprises depositing or bonding bumps or balls to the terminal bonding sites.

64. A system comprising:

a substrate; and

a semiconductor component on the substrate comprising a chip on board leadframe comprising a plurality of leadfingers a plurality of interconnect bonding sites on the leadfingers, and a plurality of terminal bonding sites on the leadfingers in an area array, a semiconductor die back bonded to the leadfingers, a plurality of interconnects bonded to the die and to the interconnect bonding sites, a plurality of terminal contacts on the terminal bonding sites, and an encapsulant encapsulating the die, the interconnects and the leadframe.

65. The system of claim 64 wherein the substrate comprises a module substrate and the system comprises a multi chip module.

66. The system of claim 64 wherein the substrate is contained in a computer.

67. The system of claim 64 wherein the substrate is contained in a camcorder.

68. The system of claim 64 wherein the substrate is contained in a camera.

69. The system of claim 64 wherein the substrate is contained in a cell phone.

70. A system comprising:

a substrate comprising a plurality of electrodes; and

a semiconductor component on the substrate comprising:

a leadframe having a first side, an opposing second side, an inner portion and an outer periphery, the leadframe comprising a plurality of leadfingers;

a plurality of interconnect bonding sites on the leadfingers on the first side located proximate to the outer periphery;

a plurality of terminal bonding sites on the leadfingers on the opposing second side in an area array;

at least one bus bar electrically connecting selected leadfingers located proximate to the inner portion;

a semiconductor die back bonded to the leadfingers on the first side;

a plurality of interconnects bonded to the die and to the interconnect bonding sites; and

a plurality of terminal contacts on the terminal bonding sites bonded to the electrodes on the substrate.

71. The system of claim 70 wherein the system comprises a multi chip module, a computer, a camcorder, a camera or a cell phone.

72. The system of claim 70 wherein the terminal contacts comprise metal bumps or balls.

73. The system of claim 70 wherein the leadframe has a chip on board configuration.

74. The system of claim 70 wherein the interconnects comprise wire bonded wires.

75. The system of claim 70 wherein the component has a chip scale outline.